In the Claims

CLAIMS

Claims 1-75 (Canceled).

76. (Currently amended) A thin film transistor comprising:

a variable thickness thin film transistor layer, the transistor layer having a channel region elongated in an upward direction and one of a source region or a drain region elevationally above the channel region, the one region comprising a structure elongated in a lateral direction substantially perpendicular to the elongated upward direction of the channel region, and the one region having a dimension in the lateral direction greater than a greatest dimension of the channel region in the lateral direction; and

a gate in lateral proximity to the ~~thin film~~ channel region, the gate comprising an annulus which laterally encircles the laterally proximate ~~thin film~~ channel region.

77. (Previously presented) The thin film transistor of claim 76, further comprising a substrate supporting the thin film transistor layer, and wherein the one region comprises the elongated structure oriented substantially parallel to the substrate.

78. (Previously presented) The thin film transistor of claim 76, wherein the source region and the drain region are oriented parallel relative to one another, the channel region is oriented substantially perpendicularly relative to both the source and drain regions.

79. (Previously presented) The thin film transistor of claim 76, wherein he source region and the drain region are provided in different elevational planes, the channel region is disposed elevationally between the source region and drain region.

80. (Previously presented) The thin film transistor of claim 79, wherein the source region and the drain region having different thicknesses.

81. (Previously presented) The thin film transistor of claim 76, wherein the channel region comprising an annulus encircled by the gate.

82. (Previously presented) The thin film transistor of claim 76, further comprising:

a first dielectric layer disposed over a semiconductor substrate;

a gate electrode layer disposed over the first dielectric layer;

a second dielectric layer disposed over the gate electrode layer and having an upper surface; and

an opening extending through the second dielectric layer, the gate electrode layer and the first dielectric layer, the opening having opposing sidewalls and a bottom disposed between the opposing sidewalls.

83. (Previously presented) The thin film transistor of claim 82, wherein the variable thickness thin film layer is disposed within the opening and extending outward from the opening and overlying at least a portion of the upper surface.

84. (Currently amended) The thin film transistor of claim 82, wherein at least some of the one region is disposed over the upper surface of the second dielectric layer.

85. (Previously presented) The thin film transistor of claim 82, further comprising a gate dielectric layer within the opening, at least a portion of the gate dielectric layer is elevationally coincident gate electrode layer.

86. (Previously presented) A thin film transistor comprising:

a variable thickness thin film transistor layer supported over a substrate, the transistor layer having a thin film channel region, a first thin film source/drain (S/D) region and a second thin film S/D region, the first S/D region extending laterally in an elongated direction substantially parallel to surface of the substrate and having an elongated dimension greater than a greatest dimension of the second S/D region structure in a direction parallel to the surface of the substrate; and

a gate in lateral proximity to the thin film channel region, the gate comprising an annulus which laterally encircles the laterally proximate thin film channel region.

87. (Previously presented) The thin film transistor of claim 86, wherein the first thin film S/D region is disposed elevationally above the thin film channel region.

88. (Previously presented) The thin film transistor of claim 87, wherein the thin film channel region comprises an elongated structure oriented substantially perpendicularly relative to the elongated structure of the first thin film S/D region.

89. (Previously presented) The thin film transistor of claim 86, wherein the first thin film S/D region and the second thin film S/D region are oriented parallel relative to one another, and wherein the thin film channel region is oriented substantially perpendicularly relative to both the first and second thin film S/D regions.

90. (Previously presented) The thin film transistor of claim 86, wherein the first thin film S/D region and the second thin film S/D region are provided in different elevational planes, the channel region is disposed elevationally between the first and second thin film S/D regions.

91. (Previously presented) The thin film transistor of claim 86, wherein the first thin film S/D region is provided elevationally above the second thin film S/D region.

92. (Previously presented) The thin film transistor of claim 86, further comprising:

a first dielectric layer disposed over a semiconductor substrate;

a gate layer disposed over the first dielectric layer;

a second dielectric layer disposed over the gate layer and having an upper surface; and

an opening extending through the second dielectric layer, the gate layer and the first dielectric layer, the opening having opposing sidewalls and a bottom disposed between the opposing sidewalls, the thin film transistor is disposed within the opening and over the upper surface.

93. (Previously presented) The thin film transistor of claim 92, wherein the first thin film S/D region is provided having at least a portion overlying the upper surface and the second thin film S/D region, and wherein the second thin film S/D region is provided having at least a portion overlying the bottom of the opening.

94. (Previously presented) The thin film transistor of claim 92, further comprising a gate dielectric layer disposed within the opening adjacent the opposing sidewalls, where the thin film transistor layer is disposed over the gate dielectric layer.

95. (Previously present d) The thin film transistor of claim 94, wherein the gate dielectric layer is an annulus received in the opening, the annulus having a top disposed elevationally below the upper surface.

96. (Currently amended) A thin film transistor comprising:

a first dielectric layer disposed over a semiconductor substrate;

a gate electrode layer disposed over the first dielectric layer;

a second dielectric layer disposed over the gate electrode layer and having an upper surface, wherein the gate electrode layer and the second dielectric layer comprise an opening extending from the upper surface to the semiconductor substrate, the opening defining opposing sidewalls in the gate electrode layer;

a gate dielectric layer disposed over a portion of the sidewalls as an annulus, the annulus having a top that does not extend elevationally above the upper surface; and

a channel region disposed within the opening, operably adjacent the gate dielectric layer.

97. (Previously presented) The thin film transistor of claim 96, further comprising one of a first diffusion region and a second diffusion region disposed over the upper surface and the channel region.

98. (Previously presented) The thin film transistor of claim 96, further comprising one of a first diffusion region and a second diffusion region disposed over the upper surface and the channel region and the other of the first diffusion region and the second diffusion region disposed elevationally below the channel region.

99. (Previously presented) The thin film transistor of claim 96, wherein the channel region essentially fills the opening.

100. (Previously presented) The thin film transistor of claim 96, wherein the channel region essentially fills the opening and further comprising one of a first diffusion region and a second diffusion region disposed over the upper surface and the channel region and the other of the first diffusion region and the second diffusion region disposed elevationally below the channel region.

101. (Previously presented) The thin film transistor of claim 96, wherein the top of the annulus is below the upper surface.

102. (New) The thin film transistor of claim 76 wherein the gate comprising the annulus comprises an opening through the gate.

103. (New) Th thin film transistor of claim 76 further comprising a bulk substrate configured to support the one region, and wherein an other of the source or drain regions is formed using the bulk substrate.

104. (New) The thin film transistor of claim 86 wherein the gate comprising the annulus comprises an opening through the gate.

105. (New) The thin film transistor of claim 86 further comprising the substrate wherein the first S/D region is formed over the substrate and the second S/D region is formed using the substrate.

106. (New) The thin film transistor of claim 96 wherein the opening extends through an entirety of the gate electrode layer.

107. (New) The thin film transistor of claim 96 further comprising:

the semiconductor substrate;

a first S/D region formed over the semiconductor substrate; and

a second S/D region formed in the semiconductor substrate.

108. (New) The thin film transistor of claim 96 wherein the channel region completely fills the opening.